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AF/2836

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Shen	Docket No:	TI-31777
Serial No:	09/715,694	Examiner:	Rodriguez, Isabel
Filed:	11/17/2000	Art Unit:	2836
For:	IC EXCESS CURRENT DETECTION SCHEME		

APPEAL BRIEF PURSUANT TO 1.192(c)

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450 on 2-24-04.

Tommie Chambers

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Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

The following Appeal Brief is respectfully submitted in triplicate and in connection with the above identified application in response to the Final Rejection mailed September 10, 2003, and the Advisory Action mailed December 24, 2003.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated.

RELATED APPEALS AND INTERFERENCES

Appellants legal representative knows of no appeals or interferences which will be directly affected, or have a bearing on the Board's decision.

STATUS OF THE CLAIMS

Claims 1-13 were originally filed and no claims have were cancelled. Thus, the subject matter of the instant Appeal is the final rejection of Claims 1-13.

STATUS OF AMENDMENTS

The application was originally filed with Claims 1-13. By virtue of an amendment filed on January 2, 2003 Appellants had amended Claim 1. A Response After Final was faxed on October 27, 2003, amending no claims. The Advisory Action indicated that the Response has been considered.

SUMMARY OF THE INVENTION

The present invention relates to controlling hard disk drives in particular motors.

The present invention achieves technical advantages by detecting excess current on any IC including a servo driver IC and preventing the disruptive damage which can be caused by the excess current.

Referring now to Figure 1, there is shown generally at 10 an overcurrent detection circuit according to the present invention. Current through an isolation FET (Iso FET) 12 is measured and compared with a replica Sense FET 14 at the drains thereof, with the ratio current flowing through the sensing FET 14 setting the detection threshold.

A comparator 16 compares the two drain voltages of the Iso FET 12 and the Sense FET 14, which comparator 16 in turn compares the Icc motor current with the

threshold current and responsively generates an overcurrent fault signal OC to invoke further actions by the control circuitry to responsively reduce the Icc current.

It's essential to quickly detect excess current on all servo driver IC's and to prevent the disruptive damage which could be caused by the excess current.

For reference, node N1 is at the drain of Isolation (Iso) FET 12 and is coupled to the negative input to the comparator, and node N2 is at the drain of sense FET 14 and is coupled to the positive input to the comparator.

When the excess current condition occurs (when Icc becomes larger than the threshold), the drain of Iso FET 12 will be pulled lower than the threshold set at the positive input of the comparator 16, and thus, the comparator 16 output OC will transition from low to high. An OC "HIGH' state indicates the chip draws too much current. A delay in time is advantageously added in the comparator 16 to filter out any transient current spikes through the Iso FET 12. For the servo IC, the idea is to ignore current spikes caused by the spindle driver (not shown in the figure) negative flyback during normal PWM operation, and to detect only a short from the spindle three phases to ground or any other illegal operation that draws excess current.

ISSUES

The sole issue on appeal is whether Claims 1-13 are unpatentable under 35 U.S.C. § 103 over Szepesi.

GROUPING OF THE CLAIMS

Claim 1 as contained in the attached Appendix is independently patentable.

ARGUMENTS

It is respectfully submitted that Szepesi does not disclose or suggest the presently claimed invention including the capacitor directly coupled across the drains of the first FET and the second FET.

The Examiner apparently agrees with the above position.

The Examiner alleges that it would have been obvious to one of ordinary skill in the art to eliminate the diode and low pass filter.

Applicants traverse.

The elements in question could not be removed without changing the operation of Szepesi's circuit.

Consequently, the removal of these specific elements are not obvious.

Applicants have shown the importance of comparator being directly coupled. This allows an accurate comparison of the necessary signaling.

The Examiner has suggested the introduction of additional elements which would prevent the accurate comparison of the necessary signals. In fact, the interviewing elements, namely the diode and low pass filter would change the nature of the signals, resulting in a comparison that is less accurate.

There is no indication in Szepesi that excess current in the servo driver could be detected.

The diode and low pass filter could hamper the detection of the excess current by at the very least restricting the excess current. This would hamper the detection.

It is not seen how the presently claimed invention is obvious of the applied art.

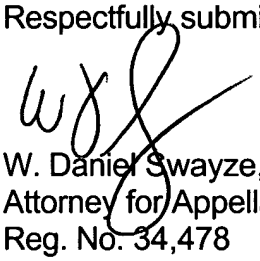
Additionally, Applicants submit that the Examiner has engaged in impressible hindsight in the modification of the Szepesi reference in order to reject Applicant's claims.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-13 under 35 U.S.C. § 103 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. **This form is submitted in triplicate.**

Respectfully submitted,



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APPENDIX

1. A overcurrent protection circuit for a motor drive circuit, comprising:

a first FET having a gate input and conducting a motor current of the motor, a drain and a source;

a second FET having a gate input coupled to said first FET input gate and conducting a bias current, a drain and a source; and

a comparator directly coupled across said drains of said first FET and said second FET and providing an output indicative of a voltage across said comparator inputs.

2. The overcurrent protection circuit of Claim 1 wherein each said first FET gate and said second FET gate are driven hard by a voltage to generate a low on resistance between the respective source and drain.

3. The overcurrent protection circuit of Claim 2 wherein said bias current is variable to responsively adjust a threshold voltage of said comparator.

4. The overcurrent protection circuit of Claim 3 wherein said second FET drain is coupled to a non-inverting input of said comparator.

5. The overcurrent protection circuit of Claim 4 wherein said first FET drain is coupled to an inverting input of said comparator.

6. The overcurrent protection circuit of Claim 2 wherein said FET drive voltage is generated by a voltage pump.

7. The overcurrent protection circuit of Claim 6 wherein said voltage pump is a voltage doubler.

8. The overcurrent protection circuit of Claim 1 wherein a ratio of said motor current to said bias current is proportional to a size of said first FET with respect to a size of said second FET.

9. The overcurrent protection circuit of Claim 1 wherein said bias current is selectively programmable.

10. The overcurrent protection circuit of Claim 9 wherein said bias current is digitally programmable.

11. The overcurrent protection circuit of Claim 1 wherein said comparator generates said output being indicative of said motor current exceeding said a predetermined threshold and being a function of said bias current.

12. The overcurrent protection circuit of Claim 1 wherein said comparator has delay circuitry filtering out any transient current spikes through said first FET.

13. The overcurrent protection circuit of Claim 1 wherein said first FET is in parallel with said second FET.